DESIGN RULES

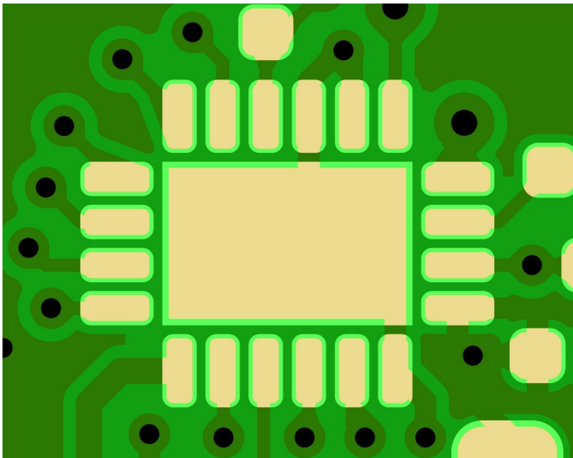
Gatema
know wow

SOLDERMASK COVERED PTH / VIA

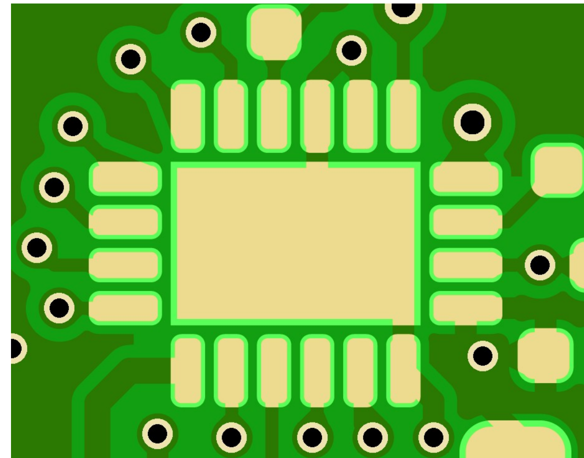
For plated-through holes with a diameter of 0.3mm or less that are covered with soldermask, there is a risk of accidental charge buildup on the surface of the pads, which can lead to a lack of gold or tin plating. This results in defects in surface finishes and a high reject rate in production, which we cannot control. There is also a possibility of chemical entrapment inside the plating, reducing the reliability of the connection.

To prevent this, it is necessary to choose one of options listed below.

1) Uncover soldermask of the plated-through holes so that process fluids can flow freely through it during manufacturing and rinsing. For this reason, all plated-through holes (<=0.3mm) must be uncovered on both sides, with the following specification: hole diameter + 100 µm
Ideally, the customer should include this adjustment in their production data, or it will be applied during data processing at Gatema PCB. If the customer disagrees with this adjustment, they must specify it in their order, but by doing so, they accept the risk of lower final surface quality associated with plated-through holes covered with soldermask or the risk of reduced reliability of the plated-through holes (not recommended).

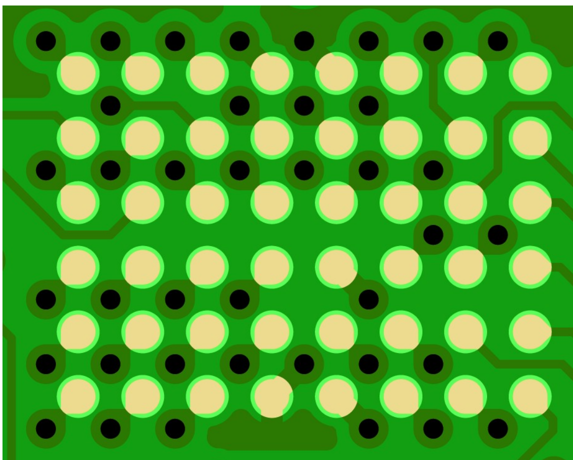


Example of via before adjustments

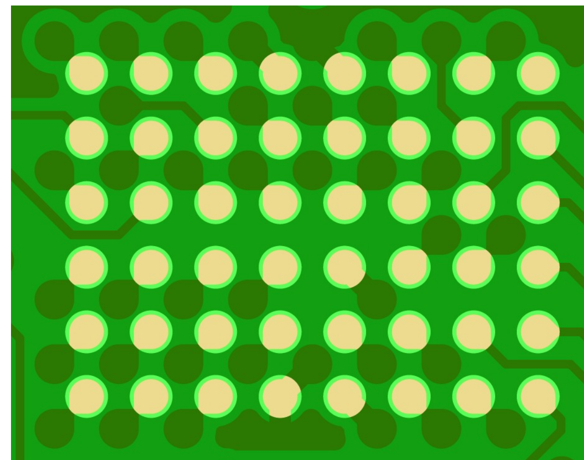


Unmasked via after adjustments

2) If the customer requires plated-through holes covered with soldermask, we recommend using via filling with overplating according to IPC-4761 Type VII.



BGA via before overplating (and filling)



BGA via covered with mask (filled and capped)